FIG. 1

BLOCK DIAGRAM SHOWING CONSTRUCTION OF FIRST EMBODIMENT
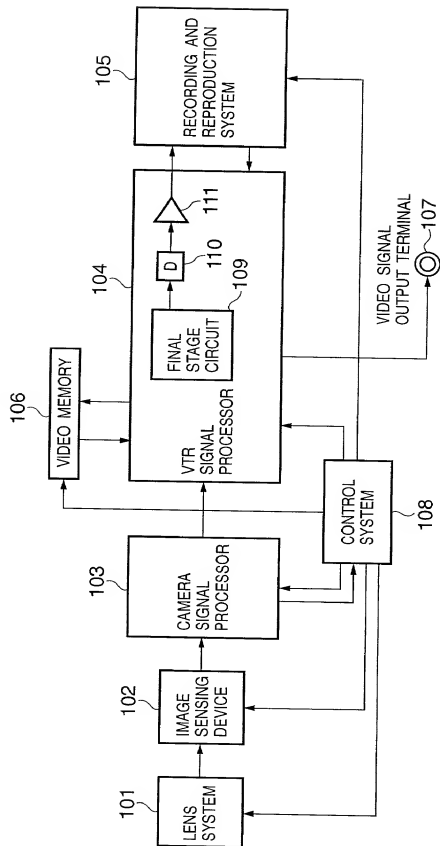
FIG. 2

TIMING CHART SHOWING OPERATION OF FIRST EMBODIMENT
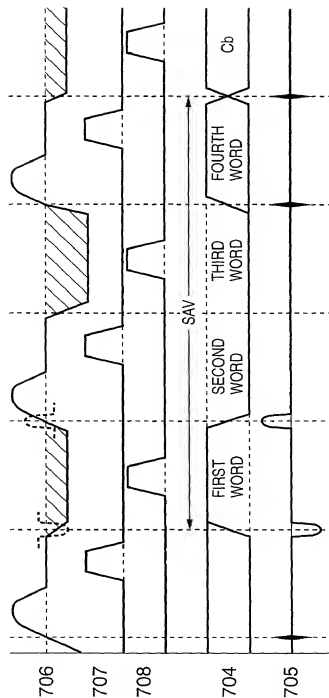

706
707
708
704
705

FIRST WORD
SECOND WORD
THIRD WORD
FOURTH WORD

SAV

Cb

F I G. 3

DIAGRAM SHOWING DELAY CIRCUIT IN SECOND EMBODIMENT

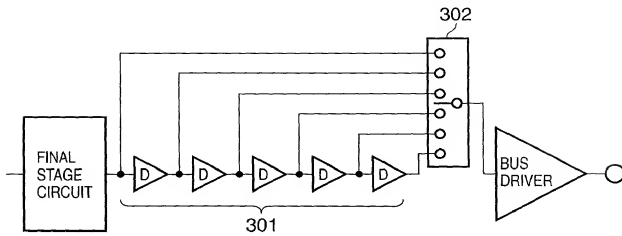# FIG. 4

EXPLANATORY VIEW OF RECORDING FORMAT CCIR Rec 601

4 : 2 : 2 : I/F (IN CONFORMITY WITH CCIR Rec 601 / SMPTE 125M)

H BLANKING

V BLANKING

FIELD - 1

V BLANKING

FIELD - 2

525 (625)

525 SD RECORD-ING
625 SD RECORD-ING

SAV (H=0)
EAV (H=1)

(525) 32 244   1440 WORDS
(625) 24 264   1440 WORDS ←—NUMBER OF WORDS AT 27MHz CLOCK

VIDEO DATA

EAV   SAV

Cb Y1 Cr Y2

Cb AND Cr : CHROMA SIGNALS AT POINT Y1
NO CHROMA SIGNAL AT POINT Y2
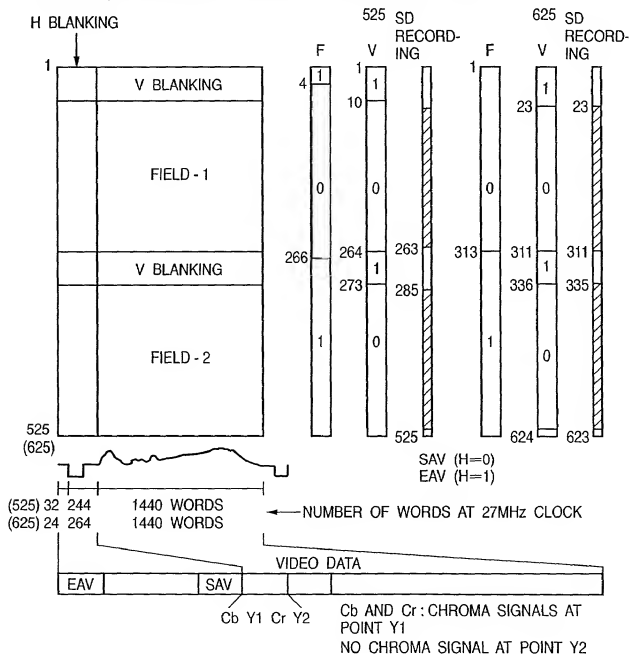
F I G. 5

EXPLANATORY VIEW OF RECORDING FORMAT CCIR Rec 601

CONTENTS OF EAV, SAV

	MSB	6	5	4	3	2	1	LSB
FIRST WORD	1	1	1	1	1	1	1	1
SECOND WORD	0	0	0	0	0	0	0	0
THIRD WORD	0	0	0	0	0	0	0	0
FOURTH WORD	1	F	V	H	P3	P2	P1	P0

F	V	H	P3	P2	P1	P0
0	0	0	0	0	0	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	0
1	0	0	0	1	1	1
1	0	1	1	0	1	0
1	1	0	1	1	0	0
1	1	1	0	0	0	1

00h AND ffh ARE NOT USED IN VIDEO DATA
10h (PEDESTAL LEVEL) IS USED IN OTHER POSITIONS THAN SAV AND EAV (BLANKING)
80h IS USED IN POSITIONS OF Cb AND Cr
SAV AND EAV EXIST IN ALL LINES (ALSO IN V BLANKING)
PARITY IS ALWAYS ADDED ON TRANSMITTING SIDE, AND USED ARBITRARILY ON
RECEIVING SIDE

F I G. 6

SCHEMATIC DIAGRAM SHOWING NOISE OCCURRENCE
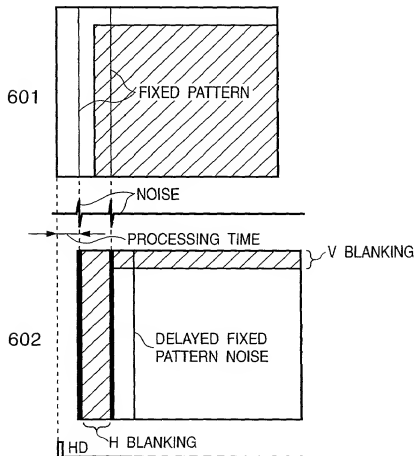POSITION IN CONVENTIONAL ART

601 — FIXED PATTERN

NOISE

PROCESSING TIME

V BLANKING

602 — DELAYED FIXED
PATTERN NOISE

HD H BLANKING

FIG. 7

TIMING CHART SHOWING OCCURRENCE AND MIXING OF NOISE
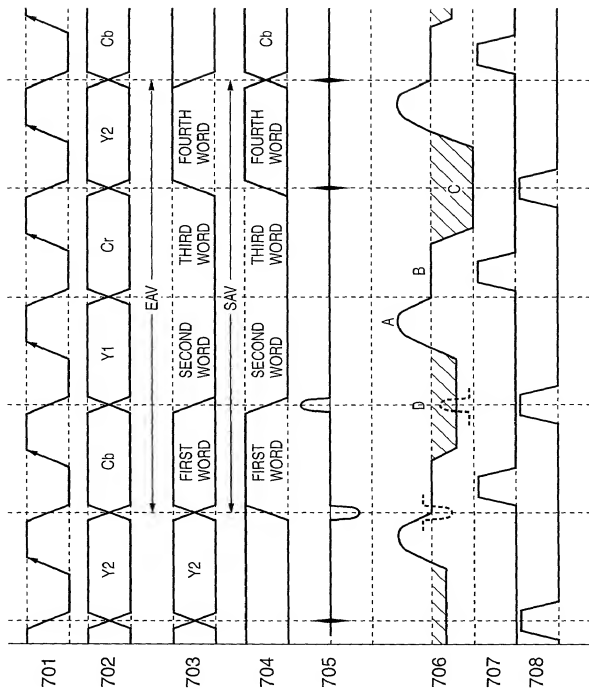
F I G. 8

BLOCK DIAGRAM SHOWING CONSTRUCTION OF CIRCUIT TO GENERATE
SYNCHRONIZING SIGNALS AND CONTROL SIGNALS

802

805

```
HORIZONTAL
PULSE
COUNTER
```

```
VERTICAL
PULSE
COUNTER
```

801

804

807

```
HORIZONTAL
PULSE
ROM
```

```
VERTICAL
PULSE
ROM
```

803

806

```
HORIZONTAL
LATCH
CIRCUIT
```

```
VERTICAL
LATCH
CIRCUIT
```

HD
HORIZONTAL DRIVE PULSE
HORIZONTAL CONTROL PULSE
ETC.

VD
VERTICAL DRIVE PULSE
VERTICAL CONTROL PULSE
ETC.

F I G. 9

BLOCK DIAGRAM SHOWING ARRANGEMENT OF PROCESSING FINAL STAGE AND
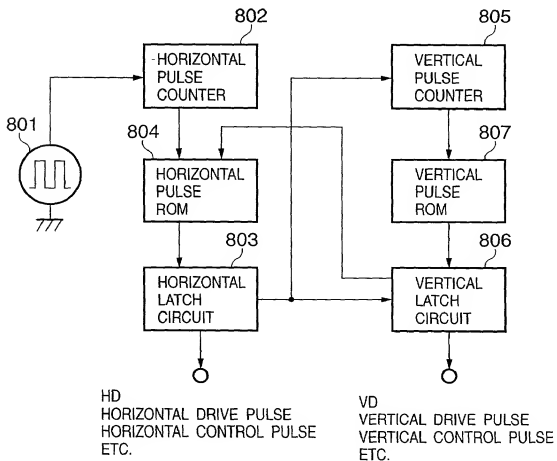PARALLEL BUS DRIVE CIRCUIT IN VTR SIGNAL PROCESSOR

VTR SIGNAL PROCESSOR (PARTIAL)

```
            ┌──────────────┬──────────────────────────┐
            │              │                          │
            │  ┌────────┐   ╲                          │
            │  │PROCESSING│   PARALLEL                  │
  ──────────┼──│ FINAL   │   BUS DRIVE  ───────────────┼──○
            │  │ STAGE   │   CIRCUIT                    │
            │  └────────┘   ╱                          │
            │      ▲                                    │
            └──────┼────────────────────────────────────┘
                   │
            ○──────┘  ADDITION OF SYNCHRONIZING
                      SIGNAL DATA
```